ABSTRACT OF THE DISCLOSURE

A memory characterization system and method using a hierarchically-stitched netlist generation technique. A plurality of leaf cells forming a memory instance are generated based on a minimum area required to encompass an optimal number of memory strap points relating to global signals that span the memory instance. Input and output pins are defined for each tile with respect to the global signals in both horizontal and vertical directions. A parametric dataset is obtained for each tile using an extractor (wherein the memory instance is in post-layout condition) or a pre-layout wire-delay estimator. The parametric netlist for the entire memory instance is assembled by coupling the individual parametric datasets using the input and output pins of the tiles with respect to the global signals.